

CLAIMS

What is claimed is:

1. A method comprising:
identifying a prefetch depth;
performing prefetching according to the identified prefetch depth; and
adjusting the performing prefetching as changes in prefetch depth are detected.
2. The method of claim 1, wherein the method further comprises, prior to identifying the prefetch depth:
querying a control register to determine whether prefetching is enabled; and
querying a data structure to identify a current prefetch depth as the identified prefetch depth if prefetching is enabled.
3. The method of claim 2, wherein querying the data structure comprising:
accessing a table, including one or more entries, defining respective prefetch depths;
identifying a table entry having a valid bit enabled; and
reading a prefetched depth from the identified table entry as the identified prefetch depth.
4. The method of claim 1, wherein prefetching comprises:
reading at least one data line from a memory according to the identified prefetch depth.
5. The method of claim 1, wherein adjusting the performing prefetching comprises:

identifying an update to a prefetch data structure;
identifying an entry within the prefetch data structure having a valid bit enabled;
reading a prefetch depth from the identified data structure entry as an updated prefetch depth; and
prefetching data according to the updated prefetch depth.

6. An article of manufacture including a machine readable medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

identifying a prefetch depth;
prefetching according to the identified prefetch depth; and
adjusting the prefetching as changes in prefetch depth are detected.

7. The article of manufacture of claim 6, wherein the method further comprises, prior to, identifying the prefetch depth:

querying a control register to determine whether prefetching is enabled; and
querying a data structure to identify a current prefetch depth as the identified prefetch depth if prefetching is enabled.

8. The article of manufacture of claim 7, wherein querying the data structure comprising:

accessing a table, including one or more entries, defining respective prefetch depths;
identifying a table entry having a valid bit enabled; and
reading a prefetched depth from the identified table entry as the identified prefetch depth.

9. The article of manufacture of claim 6, wherein prefetching comprises:
reading at least one data line from a memory according to the identified
prefetch depth.

10. The article of manufacture of claim 6, wherein adjusting the prefetching
comprises:

identifying an update to a prefetch data structure;
identifying an entry within the prefetch data structure having a valid bit
enabled;
reading a prefetch depth from the identified data structure entry as an updated
prefetch depth; and
prefetching data according to the updated prefetch depth.

11. A method comprising:
detecting a memory subsystem response level; and
adjusting a prefetch depth according to the detected memory subsystem
response level.

12. The method of claim 11, wherein the method comprises, prior to
detecting the memory subsystem response level:
determining one or more prefetch depths;
generating an entry for each prefetch depth within a prefetch data structure;
generating a validity bit entry for each respective prefetch depth entry in the
prefetch data structure; and
selecting a prefetch depth by enabling a validity bit of an entry within the
prefetched data structure corresponding to a selected prefetch depth.

13. The method of claim 12, wherein generating an entry for each prefetch depth comprises:

- selecting a prefetch depth;
- calculating a subsystem response level to activate the selected prefetch depth;
- calculating a subsystem response level to deactivate the selected prefetch depth;
- storing the activation and deactivation levels for the selected prefetch depth within a prefetch data structure entry corresponding to an entry containing the selected prefetch depth; and
- repeating the selecting, calculating the subsystem occupancy deactivation level, calculating the subsystem activation level and storing the activation and deactivation level for each selected prefetch depth.

14. The method of claim 11, wherein detecting the memory subsystem response level comprises:

- tracking memory subsystem requests; and
- tracking an average memory occupancy level as a memory subsystem response level according to the memory subsystem requests.

15. The method of claim 14, wherein tracking the average memory occupancy level comprises:

- selecting a time interval;
- summing for each clock cycle within the selected interval, a number of outstanding memory requests as a request sum; and
- dividing the request sum by a number of bus clocks within the selected interval to form the average memory subsystem occupancy level for the interval.

16. The method of claim 11, wherein adjusting the prefetching comprises:
comparing the detected memory subsystem response level to activation and
deactivation occupancy levels of one or more prefetching depths; and
selecting a new prefetching depth according to comparing of the memory of the
detected memory subsystem response level.

17. The method of claim 16, wherein selecting comprises:
comparing the detected memory subsystem occupancy level to a deactivation
occupancy level of a current prefetching depth;
selecting a lower prefetching depth if the detected occupancy level is greater
than the deactivate the occupancy level;
otherwise, comparing the detected occupancy level against an activate
occupancy level;
selecting a higher prefetch level if the detected occupancy level is less than an
activate occupancy level of the current prefetch depth; and
otherwise, selecting a current prefetch depth as the new prefetch depth.

18. The method of claim 14, wherein tracking memory subsystem requests
comprises:
determining a depth of an in order queue as the number of outstanding memory
subsystem requests.

19. The method of claim 11, wherein detecting the memory subsystem
response level comprises:
tracking subsystem memory requests; and
generating an average memory latency level as the memory subsystem response
level according to the memory subsystem requests.

20. The method of claim 19, wherein tracking memory subsystem requests comprises:

- selecting a time interval;
- summing, for each clock cycle within the selected interval, a number of outstanding memory requests as an outstanding request sum; and
- summing, for each clock cycle within the selected interval, a number of received memory requests as a received request sum; and
- dividing the outstanding request sum by the received request sum to form the average memory subsystem latency level for the interval.

21. An apparatus comprising:

- prefetch control logic to identify a prefetch depth, to prefetch data according to the identified prefetch depth, and to adjust the prefetch data as changes in prefetch depth are detected.

22. The apparatus of claim 21, further comprising:

- prefetch depth logic to detect, during prefetch of a memory subsystem response level, and to adjust a prefetch depth according to the detected memory subsystem response level.

23. The apparatus of claim 21, wherein the prefetch control logic to identify an update to a prefetch data structure, to identify an entry within the prefetch data structure having a valid bit enabled, to read a prefetch depth from the identified data structure entry as an updated prefetch depth, and to prefetch data according to the new prefetch depth.

24. The apparatus of claim 22, wherein the prefetch depth logic comprises:
memory occupancy detection logic to track memory subsystem requests, and to track an average memory occupancy level as a memory subsystem response level according to the memory subsystem requests.

25. The apparatus of claim 22, wherein the prefetch depth logic further comprises:
memory latency detection logic to track subsystem memory requests, and generate an average memory latency level as the memory subsystem response level according to the memory subsystem requests.

26. A system comprising:
a memory controller coupled to a memory; and
a processor coupled to the memory controller, the processor including:
prefetch control logic to identify a prefetch depth, to prefetch data according to the identified prefetch depth and to adjust the prefetch of data as changes in prefetch depth are detected, and
prefetch depth adjustment logic to detect, during prefetch of data, a memory subsystem response level, and to adjust a prefetch depth according to the detected memory subsystem response level.

27. The system of claim 26, wherein the prefetch control logic to identify an update to a prefetch data structure, to identify an entry within the prefetch data structure having a valid bit enabled, to read a prefetch depth from the identified data structure entry as an updated prefetch depth, and to prefetch data according to the new prefetch depth.

28. The system of claim 26, wherein the prefetch depth logic comprises:
memory occupancy detection logic to track memory subsystem requests, and to track an average memory occupancy level as a memory subsystem response level according to the memory subsystem requests.

29. The system of claim 26, wherein the prefetch depth logic further comprises:
memory latency detection logic to track subsystem memory requests, and generate an average memory latency level as the memory subsystem response level according to the memory subsystem requests.

30. The system of claim 26, further comprising:
an input/output controller coupled to the memory controller via an input/output bus.